IA-64 Architecture Announcement

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Agenda

- Announcing the IA-64 Architecture
- IA-64 Server and Workstation Focus
  - Capabilities for E-business and the Internet
  - Capabilities for Technical Computing
- IA-32 and PA-RISC Compatibility
- Summary

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IA-64 Architecture Announcement

- Most significant processor architecture advancement since the Intel 80386
  - 80386: Major extension of IA architecture - 16 bit --> 32 bit
  - Merced: New EPIC technology - 32 bit --> 64 bit
- Marked by the release of IA-64 architecture details
  - Complete details on programming model, registers, application architecture
  - Details on compatibility and software optimization
- Result of the collaboration between Intel and HP

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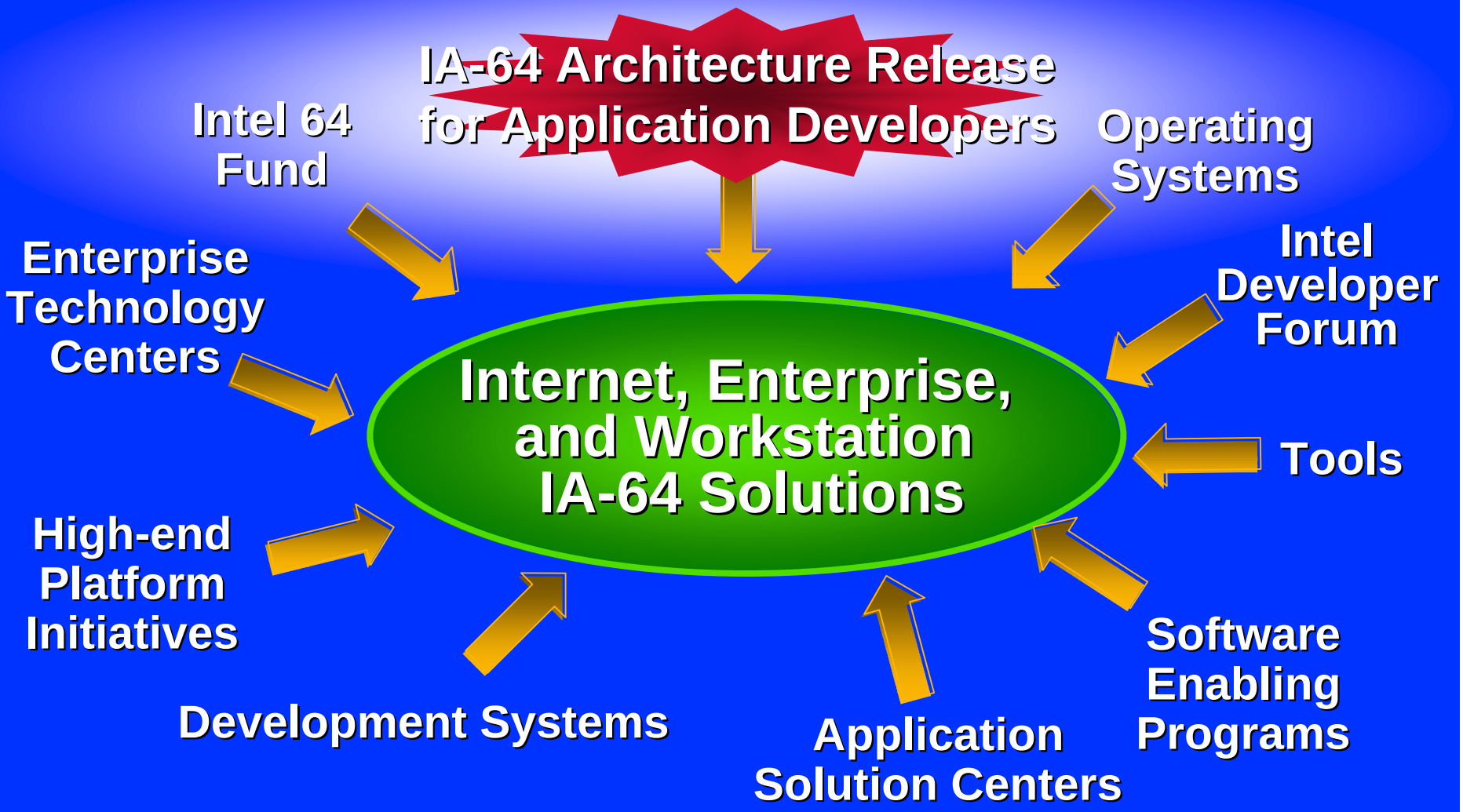
Creating Complete IA-64 Solutions



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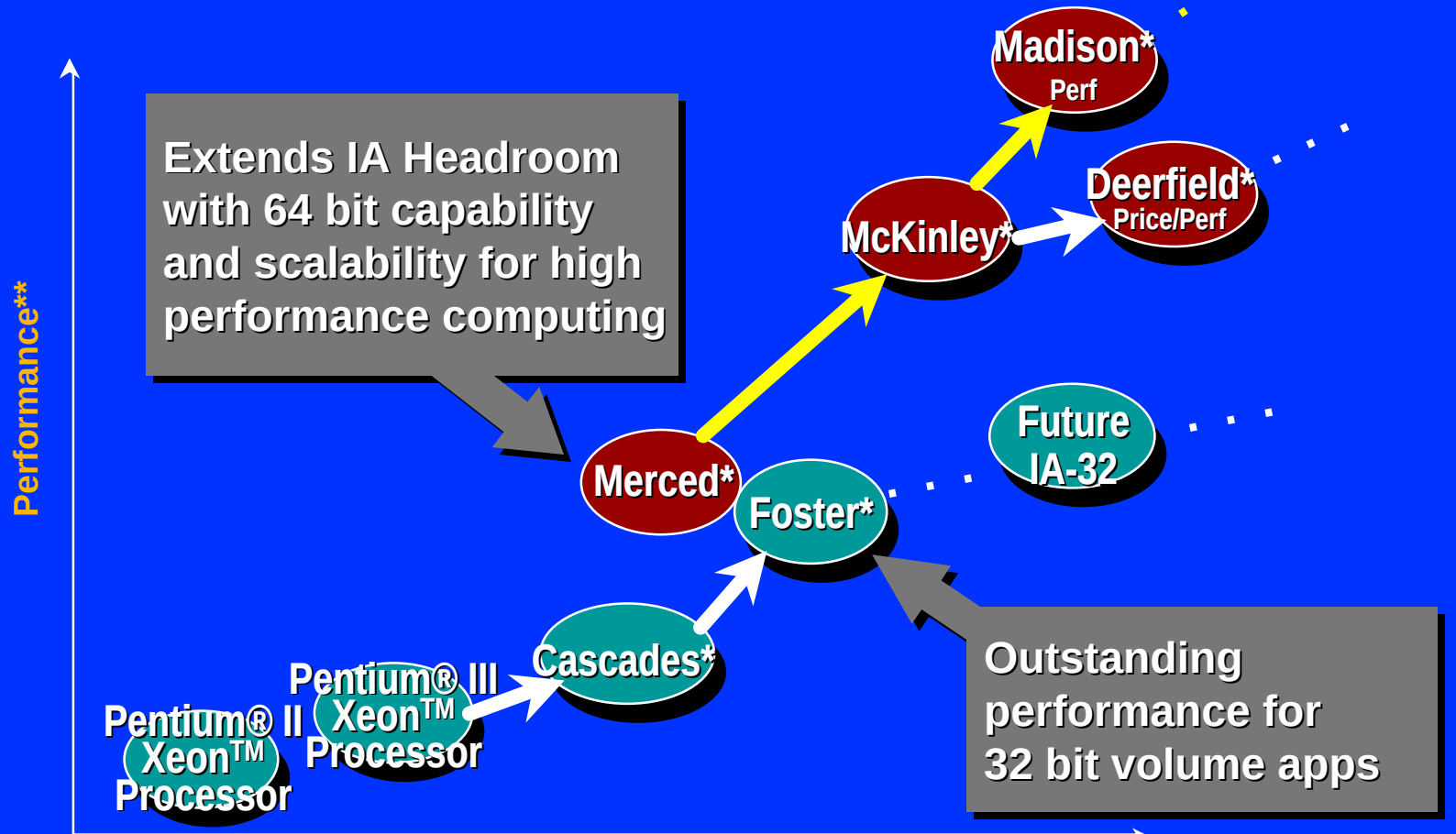
High End IA Roadmap



*Intel code name
** Not to scale

IA-32 and IA-64 Products co-exist to provide a full range of Servers & Workstations

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IA-64 Architecture Mission

- Improve upon capabilities of today's architectures
  - Effective parallelism for higher performance and scalability
  - World class floating-point for WS/scientific apps
  - 64 bit addressing for future Server and WS applications
- Designed for emerging performance intensive apps
  - Scaleable implementations : processor and system
  - Benefits for E-business, internet applications, Scientific/Financial simulation/analysis and 3D graphics
- Provide unparalleled investment protection
  - Full binary compatibility with Intel's IA-32 instruction set in processor hardware
  - Full binary compatibility with PA-RISC instructions through software translation

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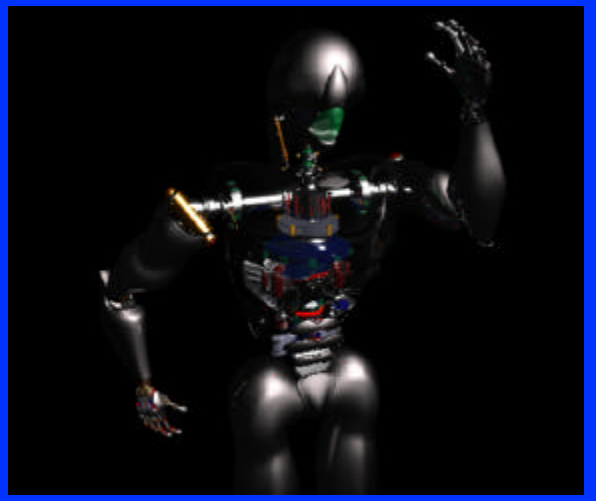
Flexible and Scalable for Emerging Applications

E-business servers
- -Large number of users
- -Large databases
- -High availability
- -Secure environment



Workstations and high performance technical computing
- -Digital content creation
- -Design engineering (EDA, MDA, etc)
- -Scientific / financial analysis

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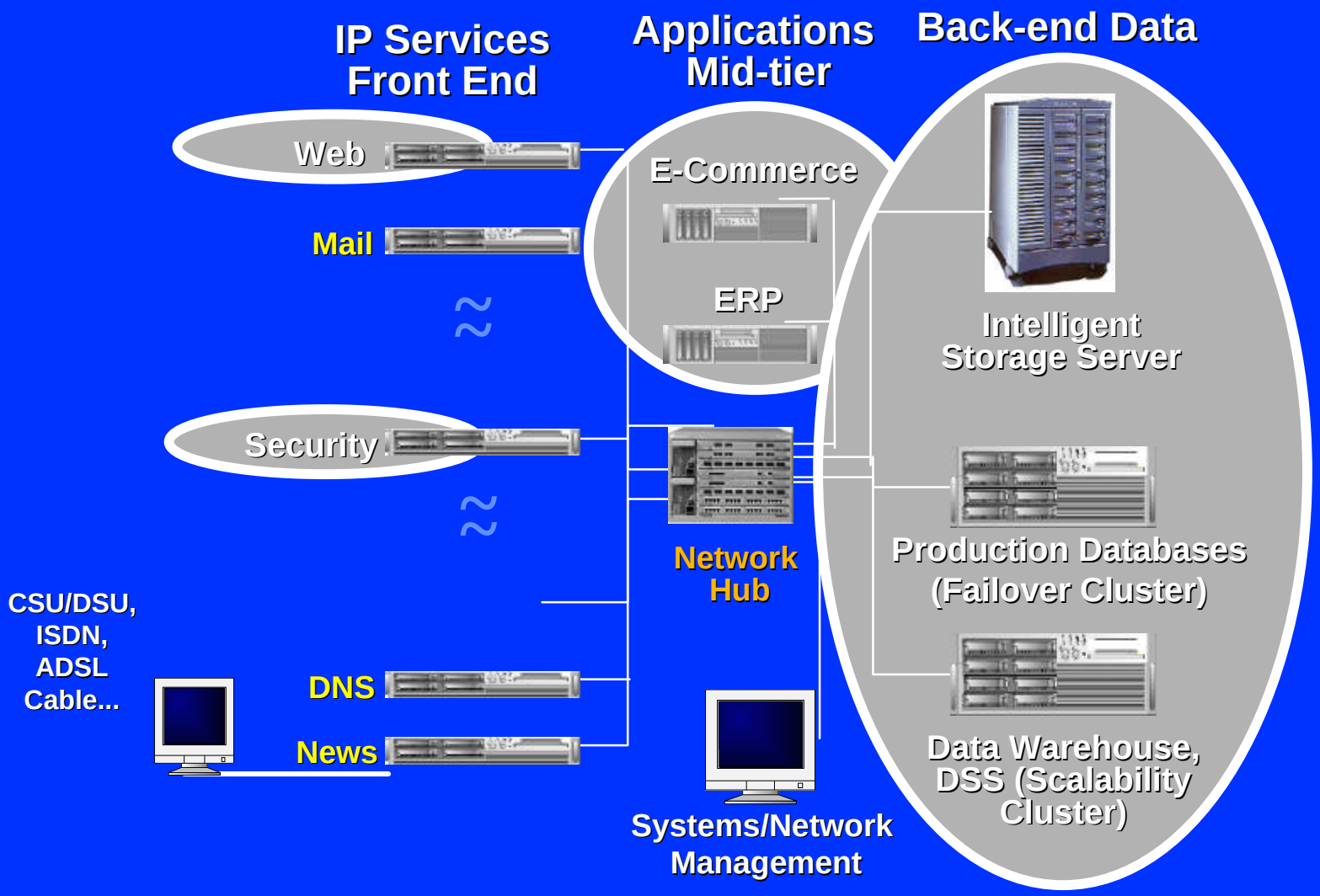
E-Business Environment

IA-64 focus area



E-business is compute-intensive requiring security and support for large databases

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IA-64 : Performance for Internet Content Delivery

- IA-64 accelerates compression / decompression of streaming media
  - Ability to execute math operations in parallel provides greater throughput
  - Configurable registers provides optimum performance on arrays of audio/video data
- Fully compatible with IA-32 MMX ä technology, Streaming SIMD Extensions and PA-RISC MAX2
  - Protects developer and end user investments

IA-64 delivers rich multimedia Web content

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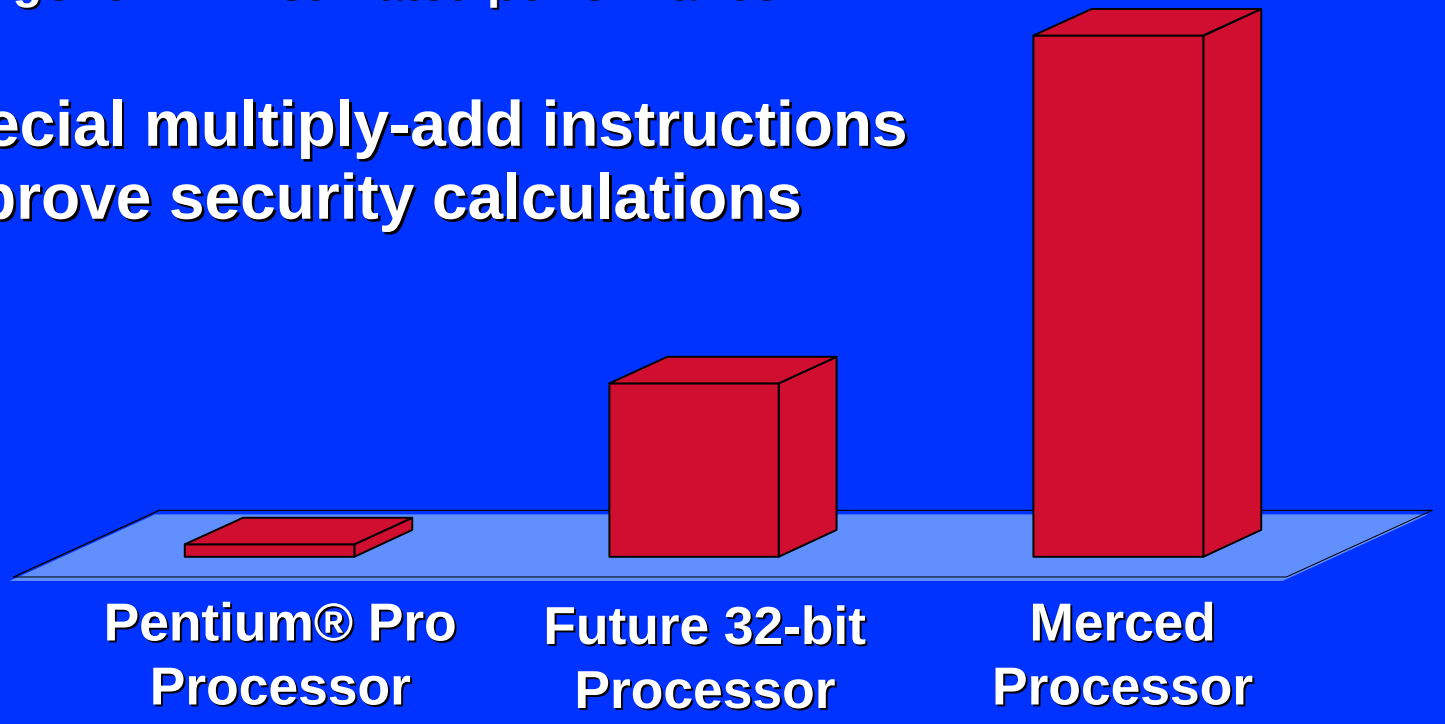
IA-64 Security Performance

RSA Algorithm – Estimated performance*

- **Special multiply-add instructions improve security calculations**



IA-64 delivers more secure transactions to more users

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**Intel estimates*

IA-64 Improves Performance for Modern Applications

- Complex mid-tier applications (ERP, etc.) have unique attributes
  - Typically written in C++, Java (object oriented)
  - Comprised of small modules which interact extensively and impact performance
- IA-64: Performance for object oriented languages
  - 256 registers provide more efficient access to data
    - Greatly reduces the need to save/store registers
    - Reduces memory/cache access requirements
  - Other features such as rotating registers and the register stack engine further improve performance

IA-64 enables more effective software optimization

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IA-64 for High Performance Databases

- IA-64 runs server applications more efficiently
  - Program decisions (branches) in large server apps overwhelm traditional processors
  - IA-64 “predication” removes branches, avoids mispredicts, improves performance
- 64-bit architecture provides scalability for future applications
  - Very large virtual and physical memory or 32 bits - as needed
  - Addresses the need for future “in-memory” databases
- IA-64 optimizes memory accesses using “speculation”
  - Reduces memory speed dependencies (latency)
  - Delivers more effective use of cache memory

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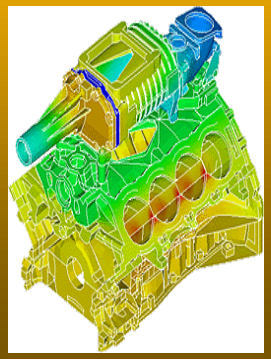
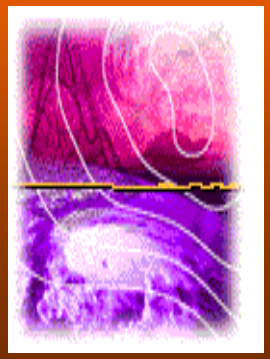
IA-64: Technical Computing

DCC	EDA	MDA	Finance	Scientific Analysis
•Rendering •Editing •3D Animation	•Verification •Synthesis •DRC	•FEA • Modeling •Hi-end CAE	•Equity •Treasury •Risk Analysis	•CFD •GIS •Molecular
				

New, Advanced IA-64 floating point architecture provides performance for technical applications

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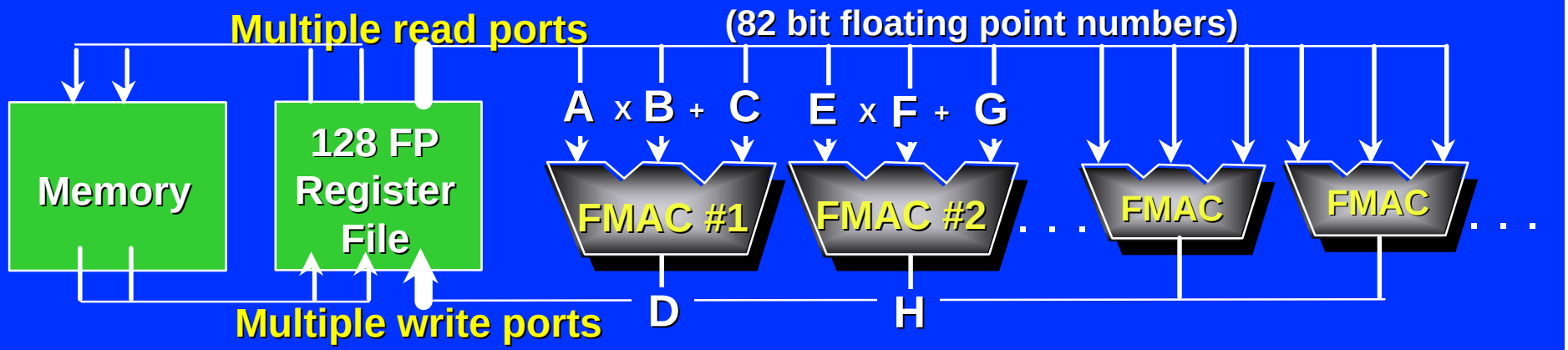
IA-64 Floating Point Architecture



- Enables world class performance : Merced ~6 GFLOPs
  - 128 floating point registers
  - Parallel execution of multiple floating point operations
- Parallel math operations benefit scientific / financial analysis
  - a * b + c = d : a single operation, multiply-accumulate (FMAC)
  - Greater precision and faster than independent multiply and add

New, optimized floating point architecture for compute intensive applications

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IA-64 Cache Management

- Cache management critical for high performance technical computing
  - Workloads are memory bound
- IA-64 pre-fetches data from memory for fast access
  - Reduces impact of memory constraints
  - Improves performance of memory intensive applications
- IA-64 manages caches for maximum efficiency
  - Special instructions allow data to be directed to optimal cache locations
  - Efficient use of caches = efficient use of bandwidth

Reduces the memory bottleneck

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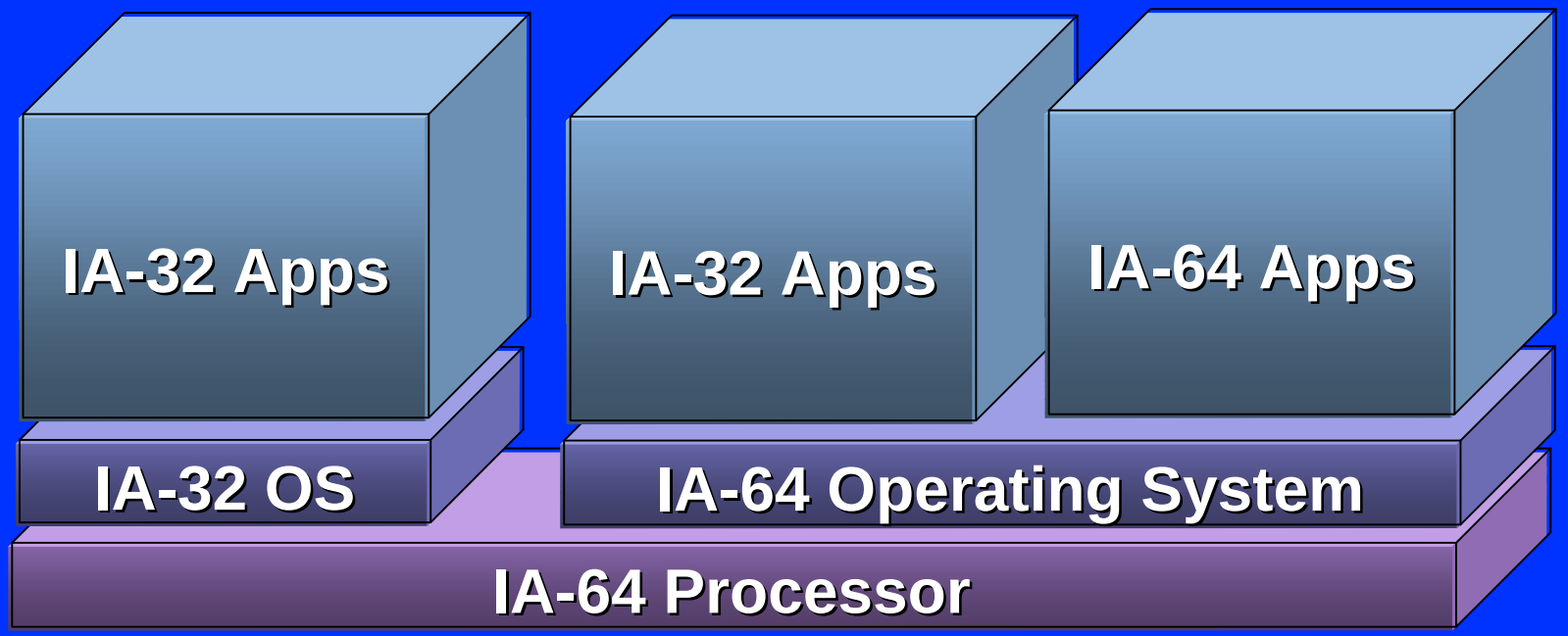
IA-64 Compatibility with PA-RISC Through Dynamic Translation

- Correctness
  - Treated as virtual microprocessor
  - Uses same tests as on PA-RISC processor
- Transparency
  - Bundled into HP-UX
  - Involved automatically when needed
- Performance
  - “Translate once, use many”
  - Optimization carries forward
  - 1:1 mapping of PA-RISC to IA-64

IA-64 Compatibility for IA-32



- Full compatibility with the IA-32 instruction set
- Includes SSE and MMX™ Technology instructions
- Supported in processor hardware

IA-64 delivers investment protection

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IA-64 : Next Generation Architecture

IA-64 Benefits	Function	IA-64 Features
• Headroom for the future	Execute more instructions in the same amount of time	EPIC : explicit parallelism, predication, speculation
• World-class performance for E-business applications	Optimized for object oriented applications (C++, Java)	Register Model : large register file, rotating registers, register stack engine
• More complex scientific / financial analysis and faster image rendering • Higher throughput of rich Internet content	High performance 3D, compression and array operations	Floating Point and Multimedia Architecture : 128 registers, parallel arithmetic, extended precision calculations, FMAC
• Increased system scalability for large applications	Large memory support, efficiently manages data flow to / from memory	Memory Management : 64-bit addressing, memory hierarchy control
• Preserves investment in existing software	Existing software runs seamlessly	Compatibility : IA-32 instructions in hardware, PA-RISC through software translation

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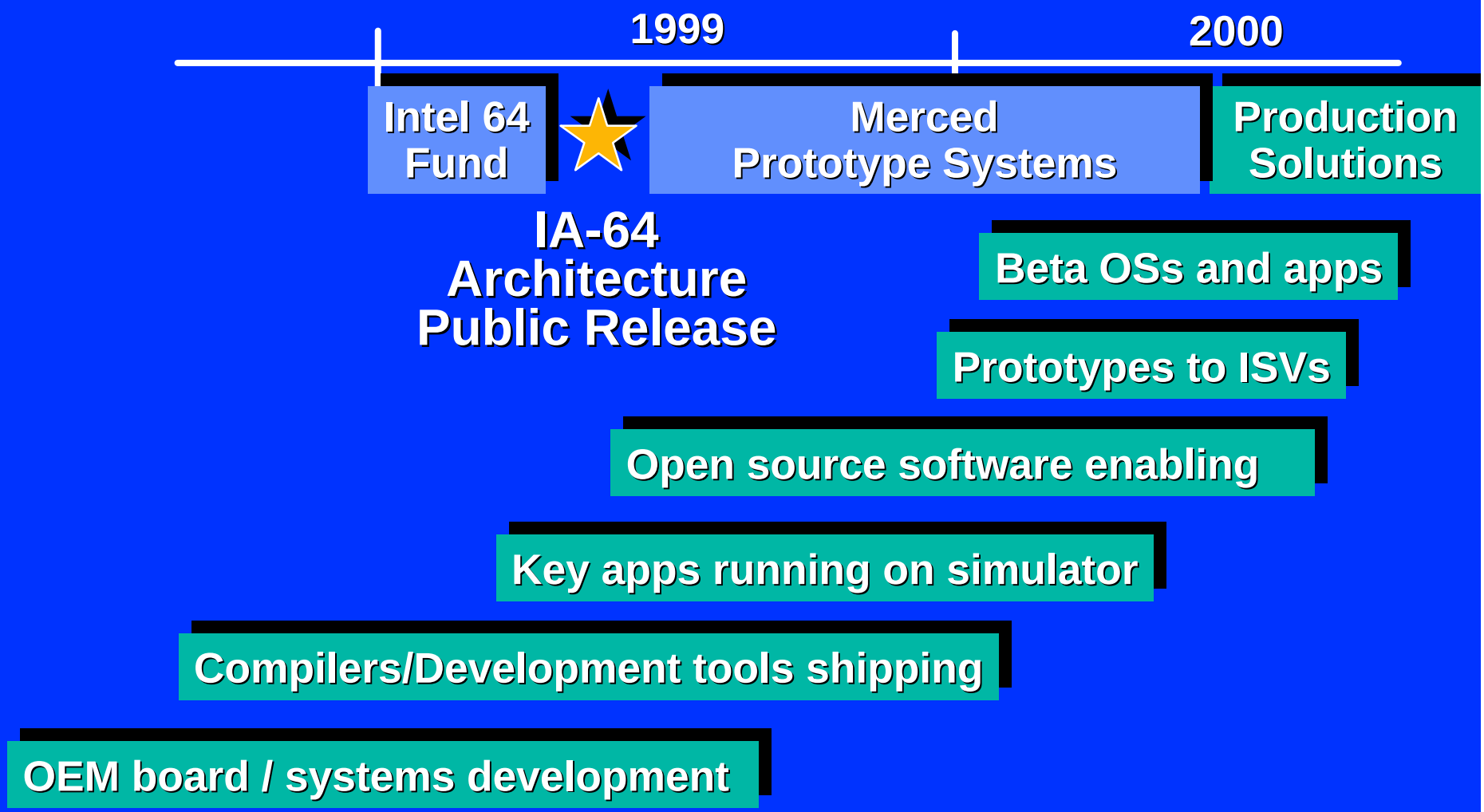
Merced Industry Rollout



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Summary

- IA-64 represents the most significant architecture development since the 80386
- IA-64 advances beyond the capabilities of traditional architectures
  - Compiler / hardware synergy, massive resources, scalability
- IA-64 provides features that benefit the performance intensive applications of the future
  - E-business and Internet applications
  - Technical computing
- Today's architecture unveiling is the next step of the comprehensive IA-64 industry program
  - Application architecture guide (AIG) available via Intel and HP websites

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Download the AIG

- http://developer.intel.com/design/ia64/index.htm
- http://www.hp.com/go/ia64

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